WHAT IS CLAIMED IS:

1. A pattern generating circuit comprising:

generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path; and

removing means for removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means.

2. A pattern generating circuit comprising:

generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path; and

removing means for sequentially removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means.

3. A pattern generating circuit as set forth in claim 2, wherein said removing means obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data.

4. A pattern generating circuit as set forth in claim 2, wherein said removing means selects a sample having the least delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

5. A pattern generating circuit as set forth in claim 2, wherein said removing means selects a sample having the most delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

6. A pattern generating circuit as set forth in claim 2, wherein said logical pattern is preliminarily generated on the basis of a coefficient set for a channel filter to be used for band restriction in said transmission path.

7. A pattern generating circuit as set forth in claim 2, wherein said logical pattern represent a peak shape in single path of the delay profile.

8. A pattern generating circuit as set forth in claim 2, wherein said logical pattern represents the peak shape and side lobe contained therein in single path of the delay profile.

9. A multi-path detection circuit for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising

generating means for generating a logic pattern of a correlated peak in said delay profile; and

detection means for detecting position of the correlated peak on the basis of the logical pattern of the correlated peak generated by said generating means.

10. A multi-path detection circuit as set forth in claim 9, wherein said detection means comprises removing means for sequentially removing power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak and means for sequentially detecting the position of said correlated peak from the delay profile by removing the power component of the correlated peak by said removing means.

11. A multi-path detection circuit as set forth in claim 9, wherein said detection means obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data.

12. A multi-path detection circuit as set forth in claim 9, wherein said detection means selects a sample having the least delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

13. A multi-path detection circuit as set forth in claim 9, wherein said detection means selects a sample having the most delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

14. A multi-path detection circuit as set forth in claim 9, wherein said logical pattern is preliminarily generated on the basis of a coefficient set for a channel filter to be used for band restriction in said transmission path.

15. A multi-path detection circuit as set forth in claim 9, wherein said logical pattern represent a peak shape in single path of the delay profile.

16. A multi-path detection circuit as set forth in claim 9, wherein said logical pattern represents the peak shape and side lobe contained therein in single path of the delay profile.

17. A multi-path detection circuit as set forth in claim 10, which further comprises position interval judgment means for detecting interval of positions of said correlated peaks and removal of power component of said correlated peak is performed by said removing means depending upon the result of judgment of said position interval judgment means.

18. A multi-path detection circuit comprising:

a matched filter outputting a correlated value of a spread code and a received signal;

delay profile storing means for storing a delay profile of a transmission path measured by said matched filter;

maximum value retrieving means for retrieving a maximum peak position and a peak level from said delay profile stored in said delay profile storing means;

pattern generating means for sequentially generating logical patterns of correlated peaks on the basis of the leak level and peak position obtained from said maximum value retrieving means; and

preparing means for preparing a profile removed a correlation power of the peak retrieved at preceding time by said maximum value retrieving means;

said maximum value retrieving means retrieves said maximum peak value and said peak level sequentially from the profile

generated by said generating means.

19. A multi-path detection circuit as set forth in claim 18, wherein said pattern generating means generates a logical pattern of the peak of preceding time on the basis of the peak level and the peak position obtained from the maximum value retrieving means,

said generating means removes correlated power detecting precedingly from the delay profile using the logical pattern of the correlated data generated by said pattern generating means.

20. A multi-path detection circuit as set forth in claim 18, wherein said maximum value retrieving means obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data.

21. A multi-path detection circuit as set forth in claim 18, wherein said maximum value retrieving means comprises

level comparing means for comparing a delay profile data samples and an interim maximum value amount retrieved samples;

selecting means for selecting one of said delay profile

data sample and said interim maximum value depending upon the result of comparison by said level comparing means;

buffer means for storing said interim maximum value during maximum value retrieval;

maximum position holding means for outputting a maximum peak position by holding a sample position upon detecting of new maximum value by said level comparing means.

22. A multi-path detection circuit as set forth in claim 21, wherein said maximum value retrieving means includes coefficient calculating means for performing calculation of a preliminarily set given value and a interim maximum value stored in said buffer means, and selecting a sample having the least delay period as a maximum point among samples on the basis of a result of calculation by said coefficient calculation means.

23. A multi-path detection circuit as set forth in claim 21, wherein said maximum value retrieving means includes coefficient calculating means for performing calculation of a preliminarily set given value and a interim maximum value stored in said buffer means, and selecting a sample having the most delay period as a maximum point among samples on the basis of a result of calculation by said coefficient calculation means.

24. A multi-path detection circuit as set forth in claim 18,

wherein said pattern generating means comprises a logical pattern memory storing a preliminarily set logical pattern, setting means for setting a peak level using a logical pattern stored in said logical pattern memory, and peak position setting means for setting a position of the correlated peak from a peak position input and peak shape output from said setting means.

25. A multi-path detection circuit as set forth in claim 18, wherein said preparing means preparing a profile removed the correlated power of the peak retrieved preceding time by said maximum value retrieving means by removing the logical pattern of the correlated peak generated by said pattern generating means from the delay profile data retrieved said maximum peak position and said peak level by said maximum value retrieving means.

26. A multi-path detection circuit as set forth in claim 18, wherein said logical pattern is preliminarily generated on the basis of a coefficient set in a channel filter used for band restriction in said transmission path.

27. A multi-path detection circuit as set forth in claim 18, wherein said logical pattern represents a peak shape in single path of said delay profile.

28. A multi-path detection circuit as set forth in claim 18, wherein said logical pattern represents a peak shape and a side lobe contained therein in single path of said delay profile.

29. A multi-lobe detection circuit as set forth in claim 18 which further comprises position interval judgment means for detecting interval of positions of said correlated peaks and priparing of profile removed said correlated power of the peak retrieved preceding time is performed by said priparing means depending upon the result of judgment of said position interval judgment means.

30 A multi-path detection method for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising the steps of:

generating a logical pattern of a correlated peak in a delay profile; and

detecting a position of correlated peak on the basis of the generated logical pattern of said correlated peak.

31. A multi-path detection method as set forth in claim 30, wherein said step of detecting position of said correlated peak position includes step of sequentially removing power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak and step of

sequentially detecting the position of said correlated peak from the delay profile removed the power component of the correlated peak.

32. A multi-path detection method as set forth in claim 30, wherein said step of detecting position of said correlated peak obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data.

33. A multi-path detection method as set forth in claim 30, wherein said step of detecting position of said correlated peak selects a sample having the least delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

34. A multi-path detection method as set forth in claim 30, wherein said step of detecting position of said correlated peak selects a sample having the most delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

35. A multi-path detection method as set forth in claim 30,

wherein said logical pattern is preliminarily generated on the basis of a coefficient set for a channel filter to be used for band restriction in said transmission path.

36. A multi-path detection method as set forth in claim 30, wherein said logical pattern represent a peak shape in single path of the delay profile.

37. A multi-path detection method as set forth in claim 30, wherein said logical pattern represents the peak shape and side lobe contained therein in single path of the delay profile.

38. A multi-path detection means as set forth in claim 31, wherein position internal of said correlated peaks are detected to remove power component of the detected correlated peak from the delay profile sequentially depending upon the result of judgment.